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Progress Report for
Seventh Quarterly Period

# R & D PROGRAM TO DESIGN AND FABRICATE DIGITAL MONOLITHIC MICROCIRCUITS HAVING AVERAGE PROPAGATION DELAY TIME OF 1 NS.

MIT, Lincoln Laboratory
Extension of Subcontract No. 295
Prime Contract No. AF 19(625)-500

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# SECTION 1 - INTRODUCTION

## 1.1 Program Objectives

This research and development program, which is an extension of M.I.T., Lincoln Laboratory Subcontract No. 295 (Prime Contract No. AF 19(625)-500) has as its primary objective the fabrication of silicon monolithic microcircuits with average propagation delay times in the subnanosecond region. A secondary objective of the program during the remaining quarterly period is to make preliminary investigation of the technological problems that relate to the fabrication of ultra high speed complex bipolar arrays. This investigation is directed toward predicting the improvements in speed that will be obtained in digital systems through the fabrication of many very high speed monolithic circuits within a single chip.

This approach is becoming mandatory as circuit time delays are approaching the time delays associated with conventional interstage wiring and capacitive loading of individual packaged circuits. The degree of success of high speed complex bipolar arrays will also depend on solutions to power dissipation, interconnection and testing problems which naturally arise from increasing microcircuit complexities and component densities.

## 1.2 Areas of Investigation

During this reporting period, primary program effort was applied in four main areas:

(1) Refinement of the techniques required for the design and fabrication of high speed npn silicon transistors.

(2) Refinement of the techniques required for the design and fabrication of digital microcircuits of the saturating and unsaturating type with better speed-power properties.

(3) Fabrication and evaluation of the SMX3, a high speed microcircuit version of an npn ECL circuit used by Lincoln Laboratory.

(4) Evaluation of the circuit design and fabrication techniques required for the construction of a complex bipolar microcircuit array for 3-bit, 9-bit, and 27-bit versions of a parity generator. The parity check system was selected in the preceding quarter as the vehicle for making a preliminary study of the problems associated with the fabrication and test of very high speed, high density single-chip microcircuits.

## SECTION 2 - FACTUAL DATA

### 2.1 Transistor Development

#### 2.1.1 0.1-Mil Geometry

During this and the previous quarterly periods, we have repeatedly demonstrated that high speed, 0.1-mil geometry transistors can be fabricated in discrete form and in monolithic microcircuits by using shallow diffusion techniques. Table 1 lists typical $f_T$ properties of various 0.1-mil geometry transistor structures that were fabricated. The data in Table 1 support the significant fact that high performance transistor designs can be incorporated into monolithic microcircuits even though the integrated circuit process adds fabrication complexity.

We recognize microcircuit arrays containing 500 to 1000 high speed, 0.1-mil geometry transistors could provide speed improvements in digital computer systems. For the fabrication of such arrays it will be increasingly important to determine and minimize those factors which adversely affect fabrication yield. In particular, it is important to determine those specific factors of 0.1-mil geometry and shallow diffusion processing which cause failure modes different that those that are encountered when the structures are made larger and deeper. These factors are expected

TABLE 1

TYPICAL TRANSISTOR PERFORMANCE

| DEVICE | EMITTER GEOMETRY<br>NO. & SIZE OF EMITTER STRIPES | BASE CONTACT GEOMETRY<br>NO.& SIZE OF BASE CONTACT STRIPES | PEAK $f_T$ (GHz) | $I_C$ @ PEAK $f_T$ (mA) |
|---|---|---|---|---|
| SMX1-T* | (2) - 0.1 x 1.5 mil | (3) - 0.1 x 1.5 mil | 2.5 - 3.0 | 10 - 12 |
| SMX2-T* | (1) - 0.1 x 0.8 mil | (2) - 0.1 x 0.8 mil | 2.6 - 3.0 | 1.5 - 2.5 |
| SMX3-T* | (2) - 0.1 x 1.5 mil | (3) - 0.1 x 1.5 mil | 3.0 - 3.5 | 10 - 15 |
| SX3** | (4) - 0.1 x 1.0 mil | (5) - 0.1 x 1.4 mil | 3.0 - 6.0*** | 15 - 20 |

*Microcircuit transistor

**Discrete transistor

***The upper limit on $f_T$ shown for the SX3 reflects the results of special fabrication techniques which have not yet been incorporated into the Integrated Circuit process.

to be primarily related to mask-making, photoengraving, diffusion, and metalization. Preliminary results of this study have indicated that of the four areas listed above, diffusion control has been a minor problem. The other process areas will be more thoroughly investigated as work proceeds on the higher density, complex bipolar parity generator array.

2.1.2 0.05-Mil Geometry

During the latter part of this quarter, the first 0.05-mil geometry (SX4) transistors were successfully fabricated. Typical devices exhibited peak $f_T$ values of 5 GHz at collector currents of 4 to 5 mA, approximately 1/4 to 1/3 the collector current exhibited by SX3 (0.1-mil geometry) transistors with comparable impurity profiles and performance. The SX4 transistor geometry (see Figure 1) is expected to provide information on the degree of transistor performance improvement that can be obtained with the high performance diffusion techniques and by reducing the device geometry as much as the present state-of-the-art will permit. It is anticipated that this type of device will be vital to the realization of very low power, very high speed, high density microcircuits.

Earlier attempts (described in subsection 2.1 of the Progress Report for the Sixth Quarterly Period) at fabricating the SX4 showed a need for refinements in the techniques then being used in

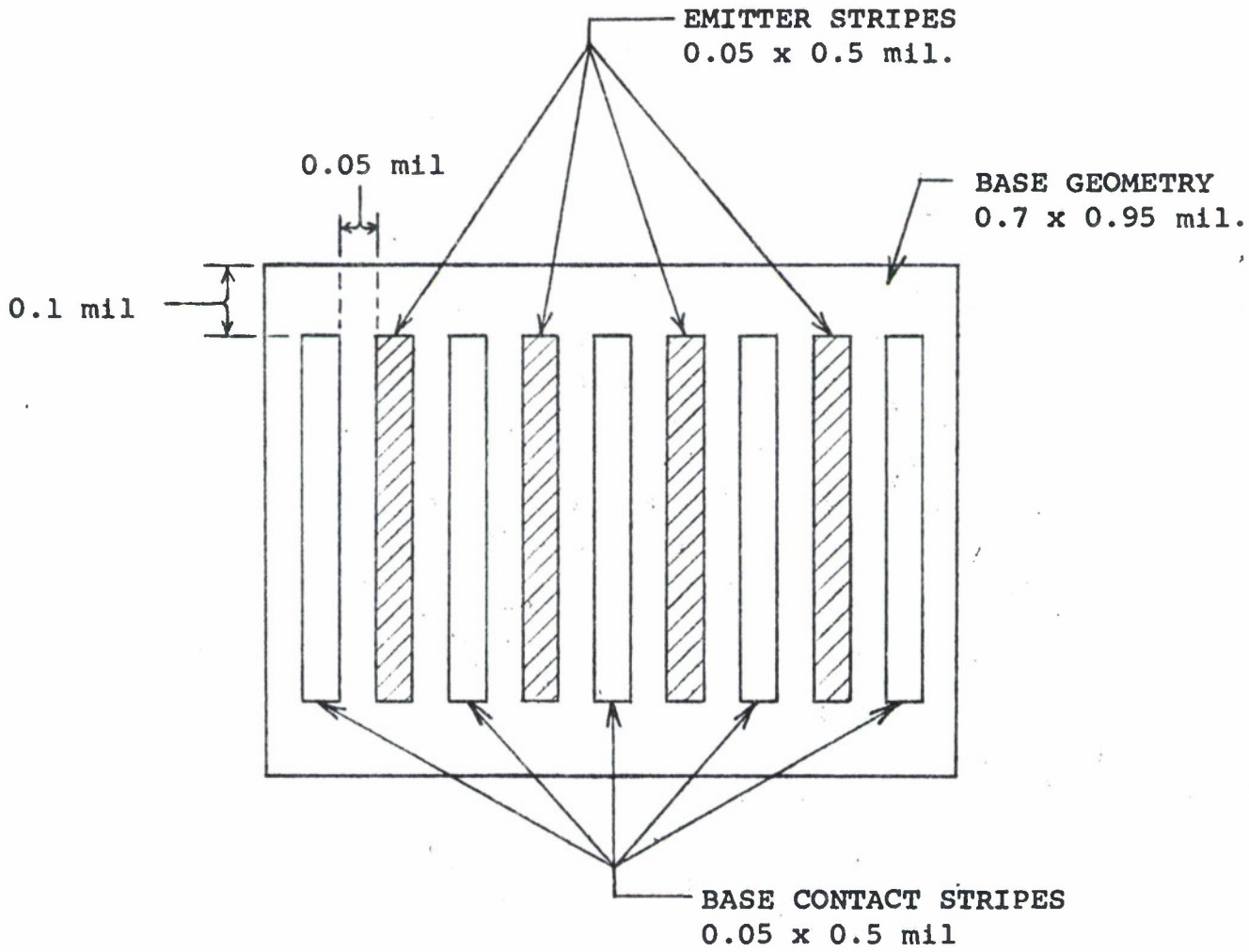



Figure 1. SX4 transistor geometry.

generating 0.05-mil photomasks. Implementation of the needed refinements not only provided the capability for demonstrating the feasibility of photoengraving 0.05-mil patterns, but also resulted in improvements in the 0.1-mil photoengraving process.

## 2.2 Microcircuit Performance Improvements

### 2.2.1 Saturating Microcircuits - TTL

SMX1 (TTL) microcircuit structures, in which n+ buried collector regions were replaced by n+ epitaxial layers in an effort to reduce residual microcircuit storage time through use of substrate transistor action, failed to show any improvement in storage time. As was predicted (paragraph 2.2.1 of the Progress Report for the Sixth Quarterly Period), the basewidth of the substrate transistor (effectively the epitaxial layer thickness) was too thick to allow proper substrate transistor action. In addition, removal of the n+ layer resulted in increased transistor $V_{CE(SAT)}$ to levels of 0.8 to 0.9 V at 1 mA $I_b$ and 10 mA $I_c$. Normal $V_{CE(SAT)}$ levels are 0.25 to 0.30 V at these currents when n+ layers are present.

Little additional work will be performed using the SMX1 microcircuit. The main reason for this is that further improvements in the $f_T$ of the inverter transistor of the circuit will have only a marginal effect on decreasing circuit propagation delay times, until means are found for reducing the storage time in saturating microcircuits.

Various techniques are being considered to reduce the circuit storage time but these will require photomask and circuit redesign, and emphasis on other program phases will probably not permit circuit fabrication. However, work planned on the SX3 (0.1-mil geometry) transistor will include evaluation of some of the techniques.

2.2.2 Non-saturating Microcircuits - ECL

SMX2 and SMX4 type ECL microcircuits were fabricated during this period. The SMX4 microcircuit is a redesigned ECL gate intended to operate at sub-nanosecond (0.1-0.2 ns) speeds and at medium power (80 mW). The first fabricated SMX4 microcircuits are currently undergoing electrical evaluation. These circuits are expected to yield the highest microcircuit speeds observed to date.

The SMX2 ECL microcircuits that were fabricated during this period were processed to obtain resistor values 2 to 3 times the original design values.

These circuit modifications reduced the power dissipation from 60 mW to 15 mW without changing the very high speed (~0.6 ns) properties of the microcircuits. This result is significant because increasing the resistor values simultaneously lowered the power dissipation and biased the transistor to a more optimum current range. The 2 to 3 increase in R-C time delays is more than offset by the speed improvements due to the factor of 2 - 3 increase in transistor $f_T$ which is obtained at the reduced bias currents.

It is equally significant that the power dissipation of this ECL circuit design compares favorably with saturated TTL circuits whereas the propagation delay time is one-half to one-third of the saturated circuit form. This result is achieved primarily through the design of higher performance transistors at reduced bias currents (see Table 1). These very encouraging results, coupled with the result of additional breadboard work, were a major factor in deciding that the ECL circuit form would be a suitable logic form for use in the parity array circuit.

Serious consideration is being given to the termination of work on SMX2 microcircuits because future efforts in the area of non-saturation microcircuits will probably be more profitably directed toward optimizing speed on the SMX4 and the basic circuit of the parity generator.

2.2.3 Parity Circuit Array

A substanital portion of the contract effort during this quarter was devoted to determining the logic form and the micro-circuit layout for a high density, high speed parity circuit array. Included in the effort were analyses of previously-made microcircuits and transistors; a paper design of the high speed, low power ECL gate to be used in the array; a discrete component breadboard study of the circuit design; and multilevel interconnection studies. Based on the results of this effort, the following decisions were made concerning the parity circuit array.

(1) The logic form to be used is ECL.

(2) The basic logic gate to be used is the 3 input gate shown in Figure 2 and designated the SMX5. A 5-stage ring oscillator constructed from microcircuit transistors similar to those to be used in the parity microcircuit, yielded average propagation delay times of 0.7 ns/stage at power levels which predict a total dissipation of 35-75 mW for the 3-bit parity system. The microcircuits themselves are expected to operate at somewhat higher speeds.

(3) Parity system array blocks of 3, 9, and 27 bits are to be fabricated containing 58, 232, and 754 components respectively. It is intended to fabricate the 3-bit parity system as a repeated cell on the wafer, and to generate through multilevel interconnection the 9 and 27-bit systems on a single silicon chip. Figure 3 is a schematic diagram of the 3-bit system.

Mask drawing and layout for the three versions of the parity system are in the early stages of preparation and should be completed during the first month of the next quarterly period.

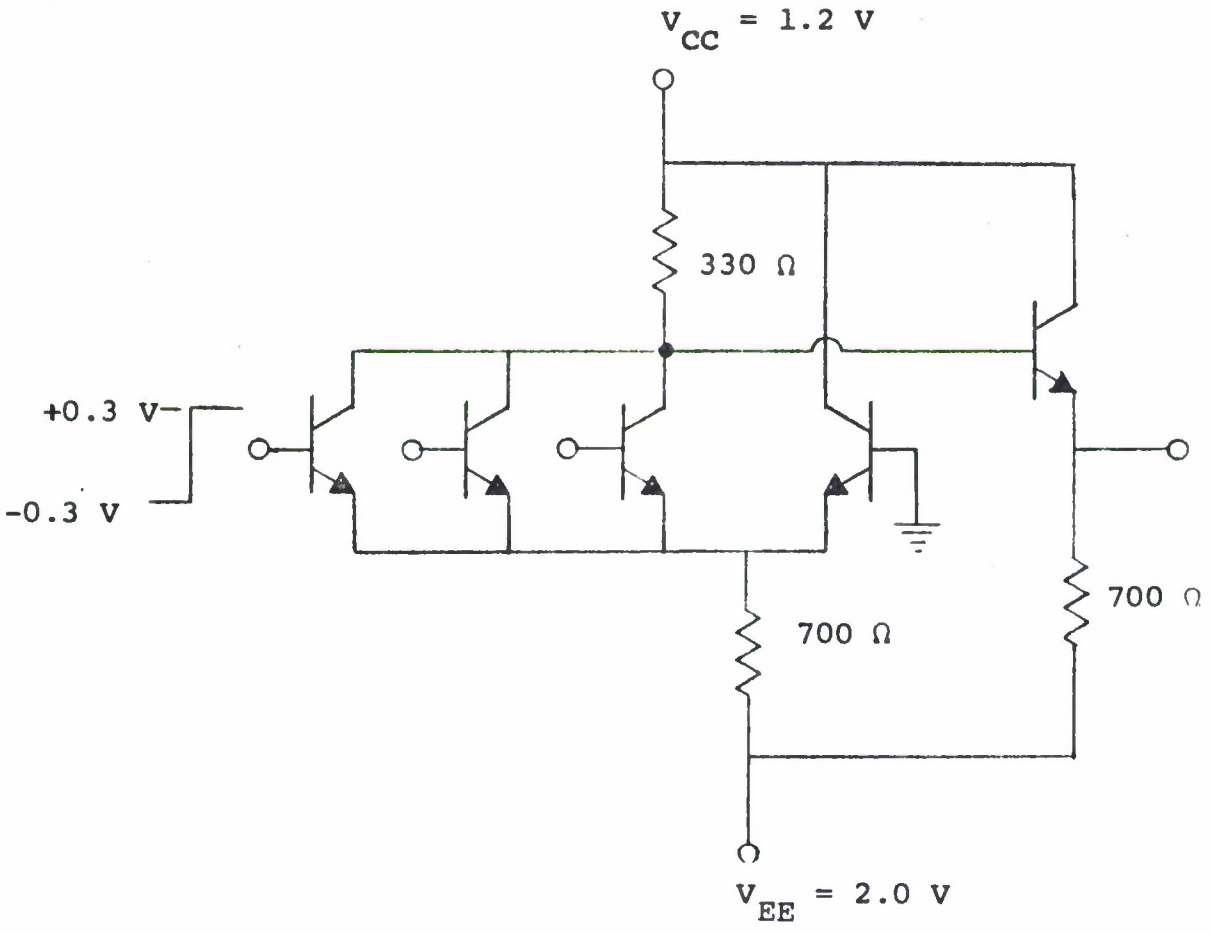



Figure 2. Basic 3-input gate for parity array.

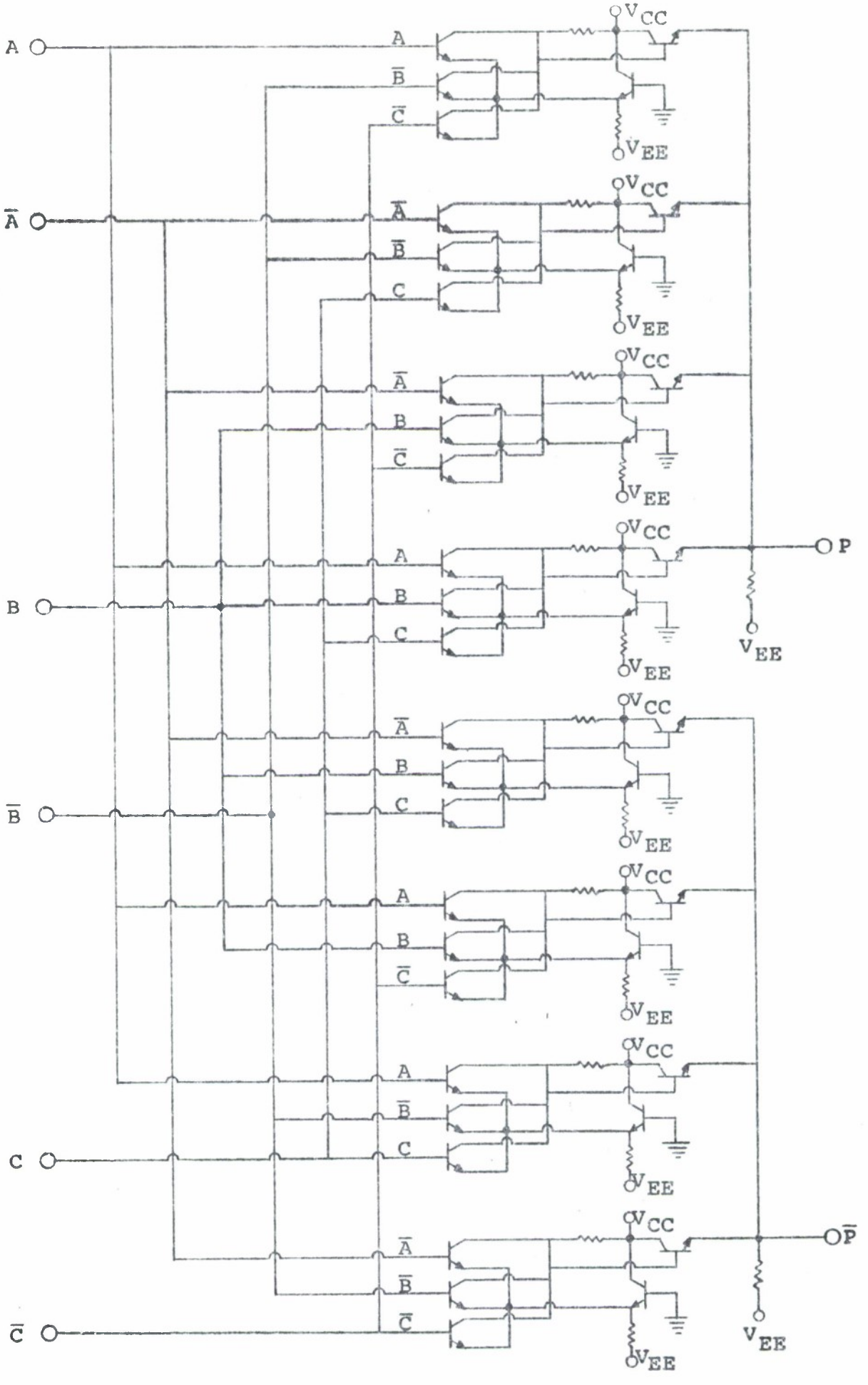



Figure 3. 3-Bit Parity Array Cell.

### 2.2.4 Fabrication of Microcircuits for Computer Circuit Evaluation

To obtain additional information on the speed advantages of monolithic microcircuits which contain very high performance transistors, an ECL type circuit (see Figure 4 ) currently being used in experimental computer circuit design by Lincoln Laboratory is being fabricated.

Two lots of SMX3 microcircuits were fabricated and tested during this quarter. Measured propagation delay times less than 1 ns were observed.

The first of the microcircuits fabricated (wafer 2B) had bias resistors lower than design value. At the prescribed bias voltage these low value resistors caused excessive collector currents to flow and resulted in saturation of the transistors. The saturation was the result of excessive voltage drop due to the large currents flowing in the transistor collector parasitic resistance.

The highest microcircuit speeds were obtained by shifting the input voltage swing from the design range of 0.0 to -1.25 V to -0.5 to -1.75 V. This prevented the collector-base diode from being forward biased and eliminated storage time delay. Under these conditions, average propagation delay times of <1.0 ns were measured.

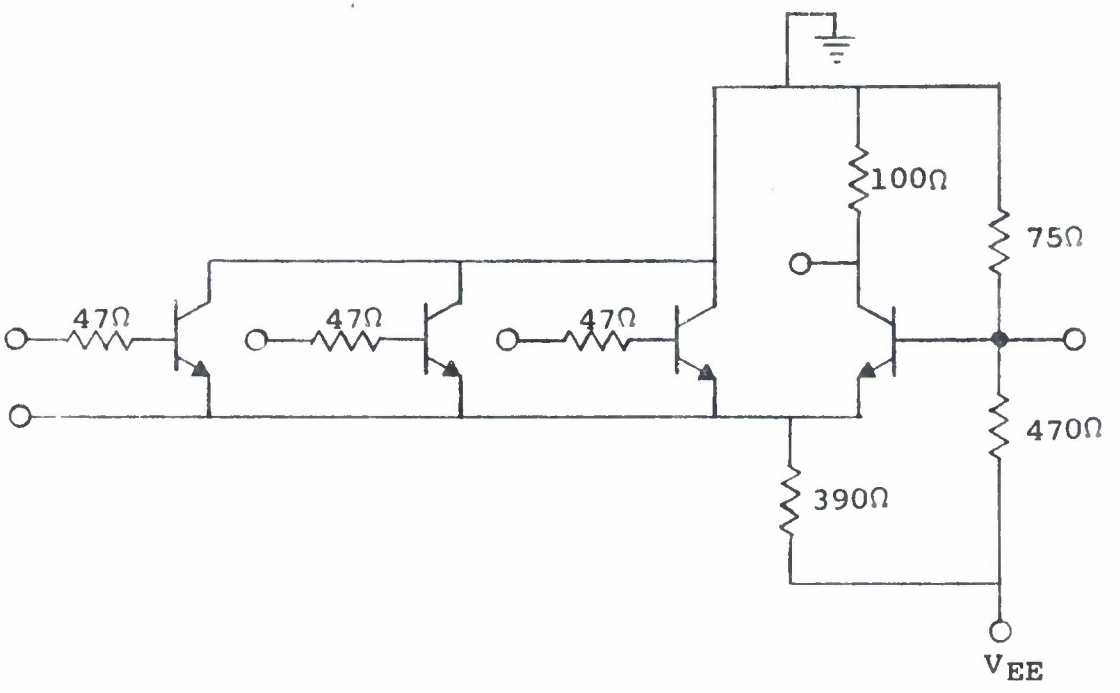



Figure 4. SMX3, Microcircuit Version of ECL Type Circuit.

Subsequent SMX3 wafers (typical of which was wafer 4A) were processed with higher value resistors. They were also gold doped to provide minimum storage time in the event of saturation with the higher value resistors. Ten microcircuits from wafer 4A will be delivered to Lincoln Laboratory. Observed propagation delay times have not been corrected for the rise and fall times of the device pulse and are probably pessimistic to the extent of 0.2 to 0.4 ns. Table 2 gives the switching data for the ten devices.

The extent of future work on the SMX3 microcircuit will be determined after Lincoln Laboratory evaluation of the 4A microcircuits.

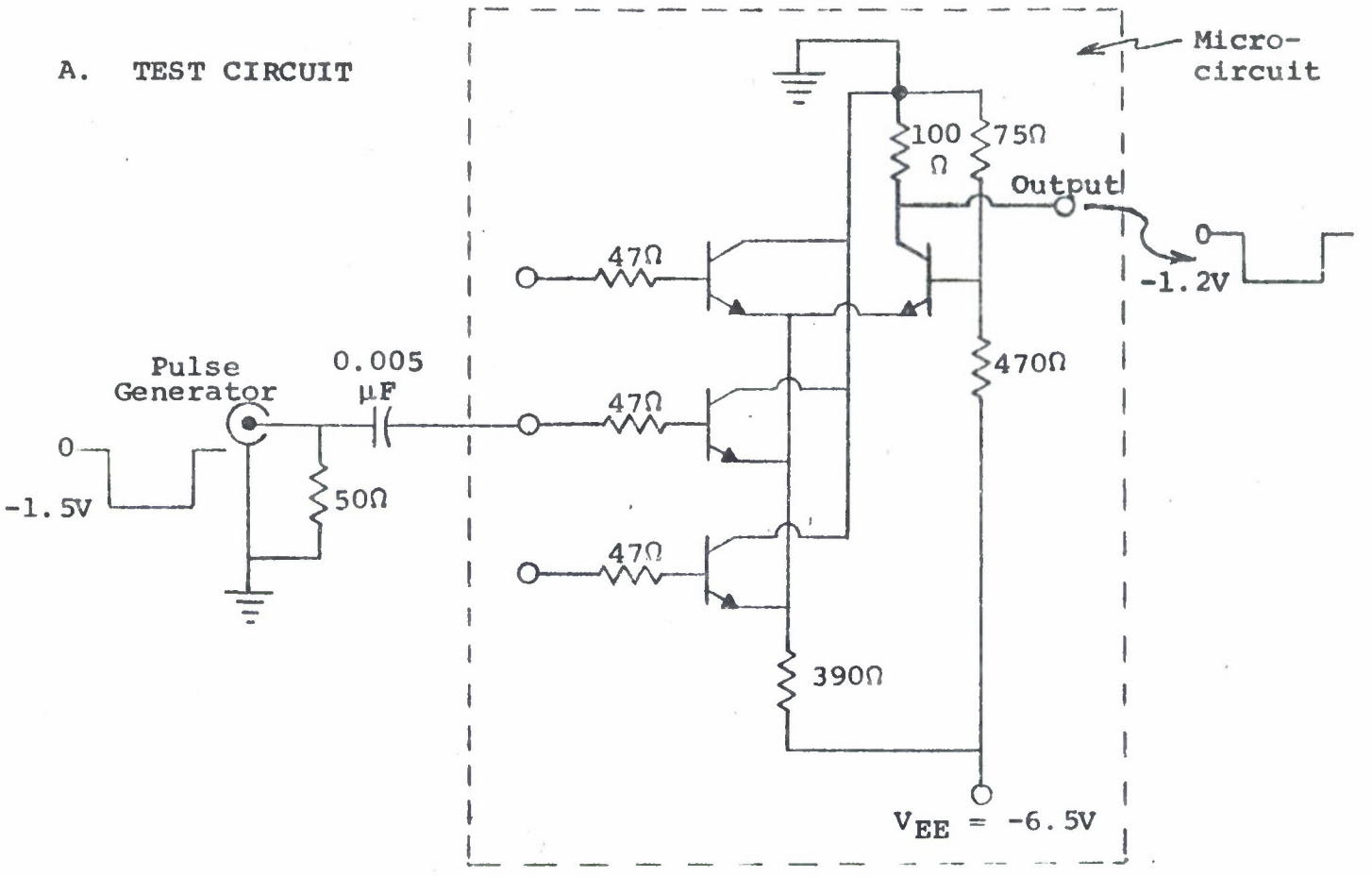
TABLE 2

A-C SWITCHING DATA FOR COMPUTER MICROCIRCUITS FROM WAFER SMX3-4A

| UNIT | GATE INPUT | $t_{off}$ | $t_{on}$ | $t_{pd}$ | UNIT | GATE INPUT | $t_{off}$ | $t_{on}$ | $t_{pd}$ |
|---|---|---|---|---|---|---|---|---|---|
| AA012 | 3 | 1.10 | 0.82 | 0.96 | AA023 | 3 | 0.95 | 0.82 | 0.89 |
| | 4 | 1.10 | 0.82 | 0.96 | | 4 | 0.98 | 0.85 | 0.92 |
| | 5 | 1.06 | 0.91 | 0.99 | | 5 | 0.93 | 0.82 | 0.88 |
| AA016 | 3 | 0.85 | 0.84 | 0.85 | AA026 | 3 | 0.94 | 0.75 | 0.85 |
| | 4 | 0.94 | 0.86 | 0.90 | | 4 | 0.95 | 0.76 | 0.86 |
| | 5 | 0.91 | 0.83 | 0.87 | | 5 | 0.96 | 0.78 | 0.87 |
| AA017 | 3 | 1.04 | 0.95 | 1.00 | AA027 | 3 | 1.23 | 0.64 | 0.94 |
| | 4 | 1.05 | 0.97 | 1.01 | | 4 | 1.22 | 0.61 | 0.92 |
| | 5 | 0.95 | 0.97 | 0.96 | | 5 | 1.18 | 0.59 | 0.89 |
| AA019 | 3 | 0.93 | 0.80 | 0.87 | AA028 | 3 | 0.90 | 0.73 | 0.82 |
| | 4 | 0.98 | 0.84 | 0.91 | | 4 | 0.93 | 0.76 | 0.85 |
| | 5 | 0.92 | 0.81 | 0.87 | | 5 | 0.94 | 0.77 | 0.86 |
| AA020 | 3 | 1.03 | 0.74 | 0.89 | AA029 | 3 | 1.15 | 0.69 | 0.92 |
| | 4 | 1.0 | 0.74 | 0.87 | | 4 | 1.18 | 0.74 | 0.96 |
| | 5 | 1.0 | 0.75 | 0.88 | | 5 | 1.08 | 0.70 | 0.89 |

These measurements were made using test procedures shown in Figure 5.

A. TEST CIRCUIT




B. TEST EQUIPMENT

Input pulses are provided by an EH 120D Pulse Generator.

Circuit waveforms and time delays are determined with a Tektronix 567 Sampling Oscilloscope which has a digital readout.

C. TIME DELAY DESIGNATIONS

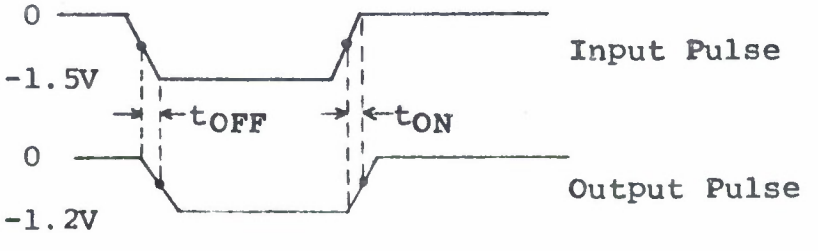



Figure 5. Testing Procedures for SMX3 Microcircuits.

## SECTION 3 - DELIVERIES OF SAMPLE DEVICES

During this quarter, the following packaged transistor and microcircuit samples were delivered to Lincoln Laboratory for evaluation.

| SAMPLE CATEGORY | SAMPLE TYPE | QUANTITY |
|---|---|---|
| Discrete Transistors | SX4* | 2 |
| TTL Microcircuits | SMX1 | 4 |
| ECL Microcircuits | SMX2 | 2 |
| | SMX3 | 12 |

* In addition to the two (2) packaged SX4 transistors, approximately nine (9) unpackaged SX4 dice were delivered to the contractor.

## SECTION 4 - WORK FOR THE NEXT PERIOD

1. Continue fabrication and evaluation of the SX3 0.1-mil geometry npn transistor.
2. Continue fabrication and evaluation of the SX4 0.05-mil geometry npn silicon transistor.
3. Continue fabrication and evaluation of the SMX4, very high speed ECL microcircuit.
4. Fabricate the parity generator.

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13. ABSTRACT

The primary objective of this research and development program is the fabrication of silicon monolithic microcircuits with average propagation delay times in the subnanosecond region. A secondary objective of the program during the remaining quarterly period is to make preliminary investigation of the technological problems that relate to the fabrication of ultra-high-speed complex bipolar arrays. This investigation is directed toward predicting the improvements in speed that will be obtained in digital systems through the fabrication of many very-high-speed monolithic circuits within a single chip. During this reporting period, primary program effort was applied in four main areas: refinement of the techniques required for the design and fabrication of high-speed npn silicon transistors and of digital micro-circuits of the saturating and unsaturating type with better speed-power properties; fabrication and evaluation of the SMX3, a high-speed micro-circuit version of an npn ECL circuit used by Lincoln Laboratory; and evaluation of the circuit design and fabrication techniques required for the construction of a complex bipolar microcircuit array for 3-, 9-, and 27-bit versions of a parity generator.

14. KEY WORDS

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digital microsystems
microcircuits
bipolar arrays